Critical Changes of EUVL

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Last week in my blog, I highlighted the progress on critical challenges of EUVL and outlined a couple of new ones that have come into focus. EUVL is now in the pilot phase and being primed by chipmakers for use in their fabs in coming years for high volume manufacturing (HVM). Although some critical challenges such as high power sources will remain on the radar in coming years, many others will be addressed by chipmakers, R&D and supplier community, as they have done to date.

The annual EUVL workshop – held in mid-June now in its sixth year – brings together R&D experts who are working on these critical EUVL challenges. In this workshop, presentations are more focused on science to deal with challenges and not on roadmaps and sales pitches. EUVL R&D topics cover a wide area – tool, source, mask, resist, contamination, optics and patterning (the second annual workshop in mid- November in Dublin, Ireland focuses only on sources) and each topic is an area of expertise in itself.

After the first EUVL workshop in 2008, the workshops' technical working group (TWG) realized the need for an overview of various technical topics and their challenges. So for the last several years, we have had excellent overview talks from experts around the world summarizing each technical field and outlining its challenges. Last year, the TWG decided that we needed to identify specific topics in each area as well, and then invite experts and authors to speak and present papers on these topics. So in this blog I would like to share the list of technical topics that has been developed with feedback from TWG members. This is a list of topics of active research. In addition, I worked with Dr. Sushil Padiyar of Applied Materials (AMAT) to develop a list of questions for a panel discussion related to EUV extendibility and its transition to 450 mm. This topic lends itself well to a panel discussion.

The proceedings from the EUVL workshop (and annual Source Workshop in Dublin) are made available at the workshop website www.euvlitho.com at no cost. I hear from people around the world on how much they use the proceedings for their research – as evident by 2,000 – 3,000 average daily hits and heavy downloads that the website receives every day. If you would like to submit an abstract for the 2013 EUVL

workshop, the deadline has been extended to March 15th and information on submissions is available at www.euvlitho.com.

List of Leading EUVL Technical Challenges

Source

- Power scaling for current Sn based DPP and LPP sources
- Physics of high power plasma and non-plasma sources (100 W - 1000 W)
- High brightness EUV sources to support mask defect metrology
- BEUV Sources (HVM and metrology) at 6.x nm
- Source requirements for high NA scanners for 10 nm and smaller nodes
- Source power requirements for 450 mm wafer scanners

Optics and Contamination

- High NA optics manufacturing
- High NA scanner design
- Thermal management for LPP normal incidence collectors
- High reflectivity BEUV optics
- Source debris management strategy
- Carbon contamination and low contamination materials and processes
- Strategies for optics contamination control

Mask

- Strategies for low defect mask blanks
- Mask technology to support high NA scanners, including transition to 9-inch masks
- Mask defect metrology: New approaches

Mask pellicles

BEUV (6.x nm) masks

Resist

Meeting simultaneous requirements for LER, sensitivity and resolution for EUV resists

Post-processing approaches to reduce LER

Resist materials and processes for the 1x node

High absorption resists

Resists materials for BEUV (6.x nm)

EUVL Panel Discussion on EUVL Extendibility and 450 mm transition

The choice of next generation lithography, beyond current 193 nm based lithography, is a critical decision for the industry. The 450 mm wafer size transition, along with HVM insertion for EUV lithography, are expected to impact the industry dynamics and cost of ownership for lithography. The panelists for this discussion are the leading lithography researchers from major semiconductor companies, who will cover topics that will include roadmaps, technical and cost requirements, and the overlap between these two major technology changes. We are looking forward to an interesting discussion by technology leaders in the industry.

List of sample questions for panelists

1. EUVL HVM Timelines

1.1 HVM Lithography roadmaps for the next 10 years for your company

1.1.1 Choice of lithography techniques for various ITRS nodes and device types

1.1.2 EUVL and 450 mm insertions for HVM

1.1.3 Lithography requirements for 300 mm and 450 mm scanners

1.2 At what node do you expect EUVL to be competitive with 193 nm immersion (193i) lithography, and for what throughput of EUVL and 193i scanners? How will this comparison differ for 300 mm and 450 mm wafers?

2 What are the EUV source requirements as a function of NA, resolution, throughput for 300 mm and 450 mm EUVL scanners?

3 450 mm and 193i Contingencies

3.1 What are your perspectives on whether 300 mm EUVL HVM will precede 450 mm wafer transition, or whether 450 mm transition will start with 193i multi-patterning and then migrate to 450 mm EUVL HVM?

3.2 What are your opinions about selections of multi-patterning EUV (13.5 nm) vs. BEUV (6.x nm) for future nodes?

This year's EUVL Workshop is scheduled for June 10-14, 2013 in Maui, Hawaii. Although the last day for submission of abstracts is now March 15, post-deadline abstracts will be accepted for poster sessions until two weeks before the workshop. Abstracts can be submitted to abstracts@euvlitho.com. Additional information about the workshop and proceedings from previous workshops are available at www.euvlitho.com.